REMARKS

The present Amendment is in response to the Examiner's Office Action mailed June 14, 2007. Claims 1, 11, 12, 13, 23, and 26 are amended. Claims 1-26 remain pending in view of the above amendments.

Reconsideration of the application is respectfully requested in view of the above amendments to the claims and the following remarks. For the Examiner's convenience and reference, Applicant's remarks are presented in the order in which the corresponding issues were raised in the Office Action.

Please note that the following remarks are not intended to be an exhaustive enumeration of the distinctions between any cited references and the claimed invention. Rather, the distinctions identified and discussed below are presented solely by way of example to illustrate some of the differences between the claimed invention and the cited references. In addition, Applicants request that the Examiner carefully review any references discussed below to ensure that Applicants understanding and discussion of the references, if any, is consistent with the Examiner's understanding.

Rejection Under 35 U.S.C. § 103

The Examiner rejected claims 1-12 under 35 U.S.C. § 103 as being unpatentable over *Kato et al.* (U.S. Patent Publication No. 2002/0021468) in view of *Casper et al.* (U.S. Patent No. 6,075,634).

The Examiner rejected claims 13-26 under 35 U.S.C. § 103 as being unpatentable over *Kato et al.* (U.S. Patent Publication No. 2002/0021468) in view of *Casper et al.* (U.S. Patent No. 6,075,634) and further in view of *Hong et al.* (U.S. Patent Publication No. 2002/0149812).

Applicants traverse the Examiner's rejection for obviousness on the grounds that the references – either individually or in combination – fail to teach or suggest each and every element of the rejected claims.

One advantage of the invention is that it allows a transceiver with an integrated circuit to communicate with a host using a serial connection. This overcomes the need to use a SERDES, which effectively multiplexes multiple parallel channels together for the transmit side and that demultiplexes channels on the receive side of the transceiver. Claim 1 has been amended to

clarify that the first electrical output port is for transmitting the retimed and reshaped first serial electrical data stream to a host that external to the integrated circuit.

Kato, in contrast, relies on the use of a DMUX 131 and a MUX 151 when communicating externally to the integrated circuit. *Kato* states that the "signal transmission process circuit 150 of the transmitting circuit unit 120 has a structure such that the data signals of 16 channels of which the transfer rates are each, for example, 622 Mb/s can be multiplexed into a multiplex data signal of 10GHz and transmitted." *See* ¶[0042]. Figure 2 illustrates that the ICs 110 and 120 include the DMUX and MUX. This teaching of requiring multiplexing and demultiplexing teaches away from the first and second serial electrical data streams required by claim 1.

Further, the loopback path taught by *Kato* is designed for separated channel signals and is only shown in Figure 2 to be connected with the demultplexed signals. *See* Figure 2; abstract. This would appear to prevent the loopback path from connecting at different places of the receive path or of the transmit path, as recited in the dependent claims, because some of these connections may not be demultiplexed or multiplexed. It does not appear to make sense to connect the loopback path between a serial stream and a multiplexer. In other words, the loopback path of *Kato* relies on a demultiplexed signal, in contrast to the requirements claim 1, which claims a flexible loopback path that is used for serial electrical data.

The Office Action further suggests that *Caspar* teaches some of the deficiencies of *Kato*. Applicants respectfully disagree. However, claim 1 has been amended to recite that the receiver eye opener circuitry components include an adaptive equalizer and a clock and data recovery (CDR). The clock from the clock and data recovery is provided to the adaptive equalizer which adaptively conditions the first serial electrical data stream.

Using both a CDR and an equalizer is not taught or suggested by the cited art. *Caspar*, for example, only teaches a gigabit Ethernet CDR and a long distance CDR. Similarly, *Kato* only suggests a clock and data recovery. The cited art does not appear to teach an equalizer and a CDR. And, as noted in the specification, the use of both the CDR and an equalizer can lead to a lower bit error rate. The use of only a CDR does not appear to achieve this advantage.

For at least these reasons, Applicants respectfully submit that claim 1 is patentable over the cited art.

Claim 11 has been amended to recite "opening an eye of the signal by conditioning the signal with an equalizer that receives a clock signal from a clock and data recovery and that equalizes the signal by removing channel noise. Claim 12 has been amended to further clarify that the equalizer adapts to channel conditions. As noted in the specification, these conditions may include changing temperature.

For at least these reasons and for the reasons previously discussed, Applicants respectfully submit that independent claims 11 and 12 and the dependent claims 2-10 are patentable over the cited art.

Claim 13 has been similarly amended and further recites a coefficient module that are used to condition the first serial electrical data stream. As discussed above, the cited art fails to disclose an equalizer and also fails to disclose a coefficient module that generates the coefficients used by the equalizer to condition the first serial electrical data stream.

Claim 23 has been amended to require conditioning the signal with an equalizer that adapts to channel conditions. Claim 26 similarly conditions the serial signal using both an equalizer and a CDR.

The cited art of *Kato*, *Hong*, and *Caspar* do not disclose an equalizer that adapts to channel conditions. *Kato* and *Caspar* may disclose a CDR, but do not disclose an equalizer that adapts to channel conditions or a coefficient module that generates coefficients used by an equalizer to condition the serial electrical signal. In other words, claims 13, 23, and 26 each require both a CDR and an equalizer. The cited art, however, may disclose a CDR.

Hong is cited as teaching a BERT. However, *Hong* does not each or suggest a BERT that is integrated in an integrated circuit as required by claim 13. Further, the BERT of claim 13 cannot be connected on the receive path and transmit path as recited in claim 13 in an integrated circuit. Rather, the BERT of *Hong* is disclosed for use in optical networks. The ability to test a test path from points on a receive path and or a transmit path are not taught or suggested by a BERT that is used in an optical network as suggested by *Hong*.

For at least for the reasons discussed herein, Applicants respectfully submit that claims 13, 23, and 26 are patentable over the combination of *Kato, Caspar,* and *Hong*. The dependent claims 14-22, and 24-25 are patentable for at least the same reasons.

CONCLUSION

In view of the foregoing, Applicants believe the claims as amended are in allowable form. In the event that the Examiner finds remaining impediment to a prompt allowance of this application that may be clarified through a telephone interview, or which may be overcome by an Examiner's Amendment, the Examiner is requested to contact the undersigned attorney.

Dated this 14th day of November, 2007.

Respectfully submitted,

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